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EXPERIMENT NO. 10

NAME OF EXPERIMENT: TO STUDY THE VERIFICATION OF LOGIC GATES (OR, AND, NOR, NAND, NOT)

APPARATUS REQUIRED

Trainer board designed for various logic gates and set of leads for connection.

THEORY

Gates are digital circuits because input and output signals have only two states either low (0) or high (1).

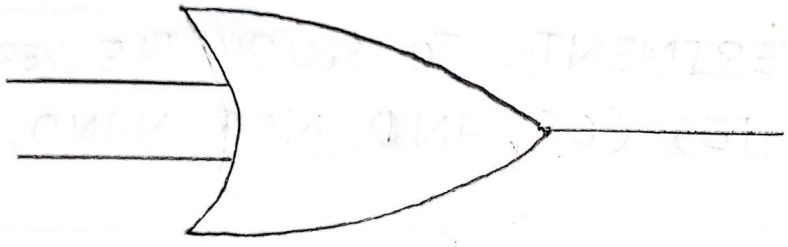
1. **OR GATE**: An OR gate has two or more than two inputs and only one output which is equal to the sum of all inputs.

Truth table

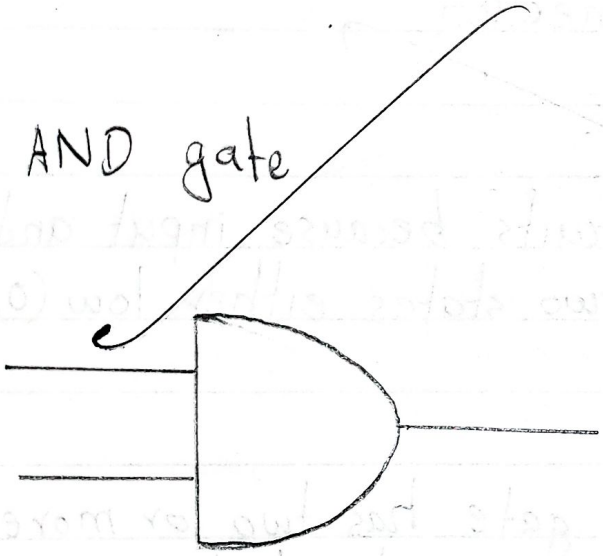
Inputs		Output
A	B	Y = A+B
low	low	low
low	high	high
high	low	high
high	high	high

Logical diagram

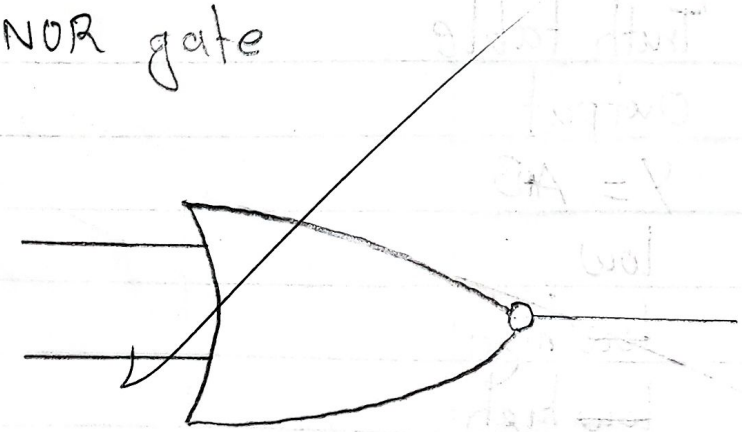
1. OR gate



2. AND gate



3. NOR gate



2. AND gate : An AND gate has two or more than two inputs and only one output which is equal to AND products of all input as shown below:

Truth Table

Inputs		Output
A	B	$y = AB$
low	low	low
low	high	low
high	low	low
high	high	high

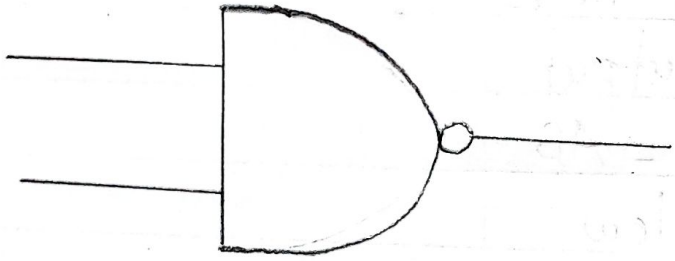
3. NOR gate : NOR gate actually means NOT-OR. It has two or more than two inputs but only one output which is the complement of the gate OR sum of two or more inputs as shown below:

Truth Table

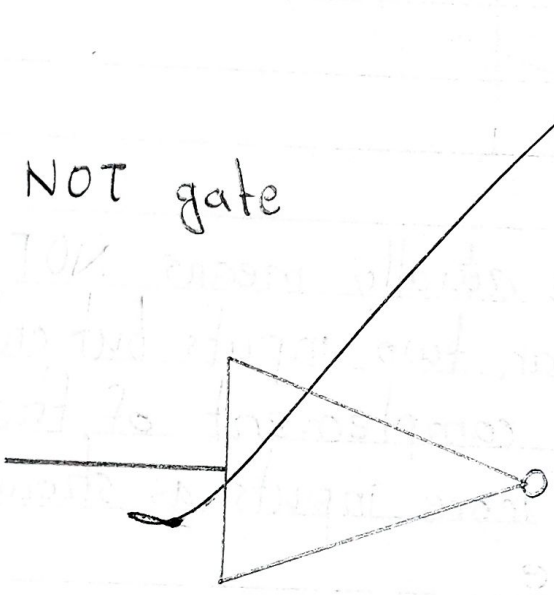
Inputs		Output
A	B	$Y = \overline{A+B}$
low	low	high
low	high	low
high	low	low
high	high	low

4. NAND gate: NAND gate actually means NOT-AND. It has two or more than two inputs but only one output which is the complement of the AND

4. NAND gate



5. NOT gate



product of all inputs as shown below:

Truth Table

Inputs		Output
A	B	$Y = \overline{AB}$
low	low	high
low	high	high
high	low	high
high	high	low

5. NOT gate: An inverter or NOT gate has only a single output and always a single input signal. Output logic is complement of input logic as shown below:

Truth Table

Inputs	Output
A	Y
low	high
high	low

PROCEDURE

1. Two ideal diodes D_1 and D_2 were connected in parallel across the output Y to make OR gate.
2. When A was at +5 V_1, D_1 was forward bias and hence conducted. The circuit current flowed via R dropping 5V across it. In this way, point Y achieved a potential of +V.

3. When +V was applied to B_1, D_1 conducted causing point Y to go to +V.
4. When both A and B were +5 V_1, the potential drop across R was 5V because of A and B were parallel. Again, point Y was driven to +5V.

Obviously, when there was no voltage either at A or B output Y is 0V. For the other gate same procedure was followed.

OBSERVATION TABLE

1. OR gate

Input		Output
A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	1

2. AND gate

Inputs		Output
A	B	Y = AB
0	0	0
0	1	0
1	0	0

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1	1	1

3. NOR gate

Inputs		Output
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

4. NAND gate

Inputs		Output
A	B	$Y = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

Inputs		Output
A	B	$Y = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

5. NOT gate

Inputs	Output
A	Y
0	1
1	0

RESULT

- For OR gate: The truth table shows that for the

OR function the output is high when any input is high.

- For AND gate: The truth table shows that for the AND function, the output is high when both inputs are high.
- For NOT gate: The truth table shows that for NOT function, the output is high when its input is low.

PRECAUTIONS

1. The circuit should be properly connected.
2. The current in the circuit should not be suddenly increased.
3. Suitable voltage and current should be applied.
4. Connected wire should be uniform, low resistivity like copper, etc.
5. Reading should be noted carefully.